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MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER
YAO, KWANG BIN

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/304,964
Filing Date: May 05, 1999
Appellant(s): CHIANG ET AL.

Alexander V. Yampolsky
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/10/02.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existance of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 5/30/02 has been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims s 2-11 and 13-18 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

US 5,771,234 Wu et al. 6-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 2-11 and 13-18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Wu et al. (US 5,771,234).

Regarding claim 2, Wu et al. discloses a system for scheduling the assignment and writing of the cells from cell sources comprising the following features: a plurality of CIU 100 in Figs. 7 and 8 including ports for receiving data cell from different data sources s_i, see column 13, lines 48-51; processor 200 in Fig. 8 for controlling the transmission of received data cells to a selected transmit port; the processor 200 including a plurality of memories, such as FIFO 110, in a plurality of CIU 100 for queuing data cells, and for receiving the data cells from the plurality of FIFO 110 in successive time slots to identify one of the output ports B', P', M', and for dynamically allocating each of the time slots controlled by TIMESLOT CLK and CLK_2 to one of the memories, such as FIFO 110, in accordance with data cells from different data sources s_i at the corresponding received ports, wherein each memory, such as FIFO 110 in Fig. 7 of each source 1, 2, 3 in Fig. 4 requests a time slot when there are cells available to be transmitted, see Fig. 4, column 9, line 43 to column 11, line 65.

Regarding claim 3, each of the queue 110 which stores each source Si in CIU 100 in Figs. 7 and 8 is assigned with at least one of the time slots in each round. See column 8, lines 8-26, and examples in Figs. 4 and 5.

Regarding claim 4, in Fig. 4, for example, during timeslot T=6, the queue in source 3 (claimed first queue) has no cell available to be transmitted; the queue source 2 (claimed second queue) has cell C7 available. Thus the timeslot 6 is allocated to the queue in Fig. 7 that stores the cell C7. See column 10, lines 26-35.

Regarding claim 5, in Fig. 4, during time slot T=7, the queue that stores cell 8 of source 2 (claimed second queue) is allocated to timeslot 7, which follows timeslot 6. See column 10, lines 36-45.

Regarding claim 6, during time slot T=8, the queue that stores cell 9 of source 1 (claimed third queue) is assigned to timeslot 8, if there is no data cell available to transmitted from source 2.

Regarding claim 7, during time slot T=9, the queue that stores cell 11 of source 1 (claimed third queue) is assigned with timeslot 9 following timeslot 8.

Regarding claim 8, Wu et al. discloses a system for scheduling the assignment and writing of the cells from cell sources comprising the following features: a plurality of CIU 100 in Figs. 7 and 8 including ports for receiving data cell from different data sources s_i, see column 13, lines 48-51; processor 200 in Fig. 8 for controlling the transmission of received data cells to a selected transmit port, such as B'_i, P'_i, M'_i; the processor 200 including a plurality of memories, such as FIFO 110, in a plurality of CIU 100 for queuing data cells, and for receiving the data cells from the plurality of memories, such as FIFO 110, in successive time slots to identify one of the output ports B', P', M', and for dynamically allocating each of the time slots controlled by TIMESLOT CLK and CLK_2 to one of the FIFO, such as FIFO 110, in accordance with data cells from different data sources s_i at the corresponding received ports; Wu further discloses the

followings: shift register 11 is checked if it has depleted the sequence of bits therein, and the cells shifted out of the FIFO 110 is output to output 0 (claimed check whether the corresponding data packet are received with an error); cells outputted to output 0 are discarded if the shift register has depleted the sequence of bits. See column 15, lines 32-41.

Regarding claims 9 and 10, Wu et al. discloses that a routing table is for lookup process, see column 2, lines 30-33. The lookup table for routing purpose is conventional. The lookup table implies that source address and destination address of the cells header compare with the entries in the lookup table, such that the cells can be routed or switched to an appropriate terminal or path.

Regarding claim 11, Wu et al. discloses that the processor 200 in Figs. 7 and 8 can determine one of the output port among ports B'_i, P'_i, M'_i for the cells received from source S_i .

Regarding claim 13, Wu et al. discloses a system for scheduling the assignment and writing of the cells from cell sources comprising the following features: placing data cells in a plurality of memories, such as FIFO 110 corresponding to the plurality of ports linked to data source S_i ; transferring the received cells stored at the plurality of memories, such as FIFO 110, in successive time slots to identify one of the output ports B', P', M',; dynamically allocating each of the time slots controlled by TIMESLOT CLK and CLK_2 to one of the FIFO , such as FIFO 110, in accordance with data cells from different data sources s_i at the corresponding received ports; wherein each memory, such as FIFO 110, representing each of the received ports is assigned with at least one of the time slots.

Regarding claim 14, Wu et al. discloses the following example depicted in Fig. 5: at timeslot 6 (claimed first time slot) is assigned to the memory corresponded to source 2 (claimed first data queue) if the memory corresponded to source 2 stored data cell C7 to be processed.

Regarding claims 15 and 16, Wu et al. discloses the following example depicted in Fig. 5: at timeslot 4 (claimed first time slot) is assigned to the memory corresponded to source 2 (claimed second data queue) if the memory corresponded to source 2 stored data cell C4 to be processed, and when there is no data in the memory corresponded to source 1 (claimed first data queue); the memory corresponded to source 2 (claimed second data queue) is assigned at the following timeslot 5 (claimed a second time slot following the first time slot) for processing data cell C5.

Regarding claims 17-18, Wu et al. disclose the following examples depicted in Fig. 4, at timeslot 3 (the claimed first times slot) is allocated to memory corresponded to source 3 (third data queue) if the memories corresponded to sources 1 and 2 (claimed first and second queue) do not stored data to be processed; at timeslot 4, the memory corresponded to source 3 is assigned with a time slot following the timeslot 3.

(11) Response to Argument

On page 12, first paragraph, Appellant argues that Wu et al. does not disclose the claimed scheduler configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry. Moreover, on second paragraph, Appellant argues that Wu et al. does not disclose the features recited in claim 2. Examiner respectfully disagrees with these arguments. Wu et al. explicitly discloses an example in Fig.4 of scheduling time slots to different memories, such as FIFO 110

in Fig.7, which store cells from respective sources S_i. The scheduling directly implies there is a request from a memory when there are data cells available for transmission. As one skill in the art can see that the scheduling for data cells is processed in 15 continuous time slots of one cycle, as depicted in Fig. 4. Each time slots is dynamically allocated to memories that must have data cells to be processed. In order to let the processor 200 know that there are available cells in the memory, the memory must inform the processor 200 so that TIMESLOT CLK and CLK_2 in Fig. 8 controlled by the processor 200 can allocate a timeslot for the memory. On the other hand, if there is no request from the memory which stores data cells, as argued by the Appellant, the processor 200 in Fig. 8 would have no idea how to allocate time slots to data memory that have data cells; thus some of the time slots might be allocated to a memory that don't have data cells to processed; in other words, there will be some empty cell timeslots in the transmission cycle. Clearly, this is not the case in the reference of Wu et al. As clearly described in the Figs. 4 and 5, and column 9-12, each timeslot of timeslots 1-15 is assigned only to the memory that have data cells to be processed. Therefore, it is respectfully submitted that Wu et al. does disclose the argued features.

On page 12, third and fourth paragraph, Appellant argues that Wu et al. does not disclose claimed ingress rules logic for receiving the data block to check whether the corresponding data packet received with an error. Examiner respectfully disagrees with these arguments. Error check of data cells is done, because shift register 11 is checked if it has depleted the sequence of bits therein, and the cells shifted out of the FIFO 110 is output to output 0 (claimed check whether the corresponding data packet are received with an error); cells outputted to output 0 are

discarded if the shift register has depleted the sequence of bits. See column 15, lines 32-41. Therefore, it is respectfully submitted that Wu et al. does disclose the argued features.

On page 13, first paragraph, Appellant argues that Wu et al. does not disclose that a data queue representing each of the receive ports is assigned with at least one of the time slots; and the reference does not disclose that a data queue representing each of the receive ports is assigned with at least one of the time slots, and one skill in the art would understand that some of the sources of Wu may be assigned with no time slots. Examiner respectfully disagrees with these arguments. First of all, these preceding arguments are misleading from the claimed invention, because the rejected claims are directed to the features of **assigning time slots to data queues** that hold data, and it is not directed to **assigning time slots to data cells from data sources** (emphasis added). As clearly depicted in Figs. 4 and 5, each memory corresponded to each data sources 1, 2 and 3 can be allocated to at least one time slot. Though some of the data cell in some timeslot (e.g., data cells C19 of data source 2 in timeslot 14 in Fig. 4) is dropped since there is no time slot available for it, the memory corresponded to that particular data source can still be assigned at different timeslots (e.g., data cells C15 of data source 2 in timeslot 11 in Fig. 4). Thus, it is believed that each memory corresponded to each data source is assigned by at least one of the time slots of one cycle, though data cells in each memory can be dropped without successfully allocated a timeslot of one cycle. Therefore, it is respectfully submitted that the features taught by Wu et al. definitely meet the intended limitations in the rejected claims.

On second paragraph of page 13, and page 14, Appellant argues that the reference does not disclose the claimed limitations in claims 3-7, 9-11 and 14-18. Examiner respectfully

disagrees with this argument. As stated in the ***Grounds of Rejection*** above, Wu et al. does disclose the each and every element in the rejected claims.

For the above reasons, it is believed that the rejections should be sustained.

KWANG BIN YAO
PRIMARY EXAMINER

Respectfully submitted,

Kwang B. Yao
November 11, 2002

Conferees
Wellington Chin
Ajit Patel